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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,929	10/02/2003	Cheng I. Sun	N1085-00154	9602

8933 7590 09/29/2004

DUANE MORRIS, LLP
IP DEPARTMENT
ONE LIBERTY PLACE
PHILADELPHIA, PA 19103-7396

EXAMINER	
KOSOWSKI, ALEXANDER J	
ART UNIT	**PAPER NUMBER**
2125	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,929	SUN, CHENG I.	
	Examiner	Art Unit	
	Alexander J Kosowski	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☒ Claim(s) *13 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1) Claims 1-33 are presented for examination.

Specification

2) The abstract of the disclosure is objected to because on line 6, the phrase "at least on" should read --at least one--. Correction is required. See MPEP § 608.01(b).

Claim Objections

3) Claims 13 and 23 are objected to because of the following informalities:

Referring to claim 13 line 2 and claim 23 line 3, there acronym "DOE" is not defined.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4) The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5) Claim 24 recites the limitation "the semiconductor manufacturing process" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7) Claims 1-3, 7-8, 10-11, 24-25, 28-29 and 31-32 are rejected under 35 U.S.C. 102(e) as being unpatentable by Tanaka et al (U.S. Pat 6,616,759).

Referring to claim 1, Tanaka teaches a method for analyzing a semiconductor manufacturing process, comprising: (a) generating sets of input and output data from the semiconductor manufacturing process (col. 3 line 50 through col. 4 line 12); (b) determining principal components from the set of input data by Principal Component Analysis (PCA) and a set of principal component score data based on the principal components (col. 5 lines 20-37); and (c) determining a relationship between the sets of input and output data from the set of principal component score data and the set of output data (col. 5 lines 38-56).

Referring to claim 2, Tanaka teaches the method of claim 1, further comprising feeding back the relationship to the semiconductor process to predict sets of new input and output data (col. 5 lines 38-56).

Referring to claim 3, Tanaka teaches the method of claim 1, wherein the step (a) comprises generating the input and output data from a thermal diffusion process (col. 3 lines 31-67, wherein thermal diffusion is a type of deposition).

Referring to claims 7-8, Tanaka teaches transforming the sets of input and output data into sets of transformed input and output data by a model, and comparing the sets of input and output data with the sets of transformed input and output data (col. 5 lines 20-56).

Referring to claims 10-11, Tanaka teaches that the step (c) comprises applying a regression model to determine the relationship, and that the regression model comprises a linear regression model (col. 5 lines 20-37).

Referring to claim 24, Tanaka teaches a system comprising at least one storing means adapted to store sets of input data and output data from the semiconductor manufacturing process (col. 3 line 50 through col. 4 line 12); and at least one processor coupled to the storing means, adapted to determine principal components from the sets of input data by Component Analysis (PCA) and a set of principal score data based on the principal components (col. 5 lines 20-37), and determine a relationship between the sets of input and output data from the set of principal component score data and the set of output data (col. 5 lines 38-56).

Referring to claim 25, see rejection of claim 2 above.

Referring to claims 28-29, see rejection of claims 7-8 above.

Referring to claims 31-32, see rejection of claims 10-11 above.

Claim Rejections - 35 USC § 103

8) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9) Claims 4-6 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, further in view of Campbell et al (U.S. PGPUB 2002/0085212).

Referring to claims 4-6, Tanaka teaches the above. However, Tanaka does not explicitly teach performing the thermal diffusion process in a vertical furnace, that the set of input data comprise different zone temperatures in the vertical furnace, nor that the set of output data comprise thicknesses of a thin film layer formed by the thermal diffusion process.

Campbell teaches a multi-zone vertical furnace which performs deposition, whereby each zone has a different temperature which is known and layer thickness is measured (Paragraphs 0009-0010).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to perform thermal diffusion in a vertical furnace consisting of multiple zones with different temperatures, and to measure layer thickness of deposited material on a semiconductor in the method taught by Tanka above since controlling temperature and measuring layer thickness in a vertical furnace would allow deposition thickness to be controlled, which would avoid costly rework of wafers due to defects and would increase manufacturing efficiencies (Campbell, Paragraph 0007).

Referring to claims 26-27, see rejection of claims 4-6 above.

10) Claims 9 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, further in view of Ruddy et al (U.S. Pat 5,064,605).

Referring to claim 9, Tanaka teaches the above. However, Tanaka does not explicitly teach that the model is an Arrhenius model.

Ruddy teaches the use of the Arrhenius model in monitored equipment (col. 4 lines 14-34).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize the Arrhenius model in the method taught by Tanaka since this model teaches the relationship between chemical reactions and temperature (Ruddy, col. 3 lines 55-61), and since it is noted that temperature is critical to a deposition process.

Referring to claim 30, see rejection of claim 9 above.

11) Claims 12-14, 17-18, 20-22 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, further in view of Schwarm (U.S. PGPUB 2004/0148049).

Referring to claim 12, Tanaka teaches the above. However, Tanaka does not explicitly teach applying design of experiment (DOE) to generate the set of input and output data.

Schwarm teaches applying DOE to generate sets of input and output data in a wafer processing system (Paragraph 0029).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize DOE to generate the set of input and output data in the method taught by Tanaka since the collected data could be used by a model generator to create a model and then the model can be used to generate process recipes for wafers (Schwarm, Paragraph 0029), and since a good DOE allows establishing a relationship between variables that may have a predictable impact on processing output while keeping the number of required experiments low (Schwarm, Paragraph 0005).

Referring to claim 13, Tanaka teaches a method comprising: (a) generating sets of input and output data from a thermal diffusion process (col. 3 line 50 through col. 4 line 12, whereby thermal diffusion is a type of deposition); (b) determining principal components from the sets of input data by Principal Component Analysis (PCA) and a set of principal component score data based on the principal components (col. 5 lines 20-37); and (c) determining a relationship between the sets of input and output data from the set of principal component score data and the

set of output data (col. 5 lines 38-56). However, Tanaka does not explicitly teach that the sets of input and output data from the thermal diffusion process are generated by DOE.

Schwarm teaches applying DOE to generate sets of input and output data in a wafer processing system (Paragraph 0029).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize DOE to generate the set of input and output data in the method taught by Tanaka since the collected data could be used by a model generator to create a model and then the model can be used to generate process recipes for wafers (Schwarm, Paragraph 0029), and since a good DOE allows establishing a relationship between variables that may have a predictable impact on processing output while keeping the number of required experiments low (Schwarm, Paragraph 0005).

Referring to claim 14, see rejection of claim 2 above.

Referring to claims 17-18, see rejection of claims 7-8 above.

Referring to claim 20, Tanaka teaches the method of claim 13, wherein the set of principal component score data comprise principal component scores (col. 5 lines 20-37, whereby a smaller number of indices is generated).

Referring to claims 21-22, see rejection of claims 10-11 above.

Referring to claim 33, see rejection of claim 12 above.

12) Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, further in view of Schwarm and Campbell.

Referring to claims 15-16, see rejection of claims 4-6 above.

13) Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, further in view of Schwarm, further in view of Ruddy.

Referring to claim 19, see rejection of claim 9 above.

14) Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, further in view of Campbell, Schwarm and Ruddy.

Referring to claim 23, Tanaka teaches a method comprising: (a) generating a set of input and output data (col. 3 line 50 through col. 4 line 12); (b) transforming the sets of input and output data into sets of transformed input and output data and (c) comparing the sets of input and output data with the sets of transformed input and output data (col. 5 lines 20-56); (d) determining principal components from the sets of input data by Principal Component Analysis (PCA) and a set of principal component scores based on the principal components (col. 5 lines 20-37); (e) determining a relationship between the sets of input and output data from the set of principal component scores and the set of output data by a linear regression model (col. 5 lines 20-37); and feeding back the relationship to the semiconductor process to predict sets of new input and output data (col. 5 lines 38-56). However, Tanaka does not explicitly teach generating a set of input data having different zone temperatures in a vertical furnace and a set of output data having thicknesses of a thin film layer by DOE, nor transforming input and output data by an Arrhenius model.

Campbell teaches a multi-zone vertical furnace which performs deposition, whereby each zone has a different temperature which is known and layer thickness is measured (Paragraphs 0009-0010).

Schwarm teaches applying DOE to generate sets of input and output data in a wafer processing system (Paragraph 0029).

Ruddy teaches the use of the Arrhenius model in monitored equipment (col. 4 lines 14-34).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to perform thermal diffusion in a vertical furnace consisting of multiple zones with different temperatures, and to measure layer thickness of deposited material on a semiconductor in the method taught by Tanaka above since controlling temperature and measuring layer thickness in a vertical furnace would allow deposition thickness to be controlled, which would avoid costly rework of wafers due to defects and would increase manufacturing efficiencies (Campbell, Paragraph 0007).

Therefore, it would also have been obvious to one skilled in the art at the time the invention was made to utilize DOE to generate the set of input and output data in the method taught by Tanaka since the collected data could be used by a model generator to create a model and then the model can be used to generate process recipes for wafers (Schwarm, Paragraph 0029), and since a good DOE allows establishing a relationship between variables that may have a predictable impact on processing output while keeping the number of required experiments low (Schwarm, Paragraph 0005).

Therefore, it would also have been obvious to one skilled in the art at the time the invention was made to utilize the Arrhenius model in the method taught by Tanaka since this model teaches the relationship between chemical reactions and temperature (Ruddy, col. 3 lines 55-61), and since it is noted that temperature is critical to a deposition process.

Conclusion

15) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander J Kosowski whose telephone number is 703-305-3958. Please NOTE that after 10/13/04, the examiner's new phone number will be 571-272-3744. The examiner can normally be reached on Monday through Friday, alternating Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 703-308-0538. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. In addition, the examiner's RightFAX number is 703-746-8370.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Alexander J. Kosowski
Patent Examiner
Art Unit 2125

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100